WHAT IS CLAIMED IS:

1. A method for evaluating reliability of a semiconductor chip structure built by a manufacturing process, comprising the steps of:

building a test structure in accordance with a manufacturing process;

thermal cycling the test structure;

measuring the yield of the test structure; and

evaluating reliability of the semiconductor chip structure built by the manufacturing process based on the yield.

2. The method as recited in claim 1, wherein the yield includes a relative number of electrically functional structures formed by the manufacturing process before thermal cycling.

3. The method as recited in claim 1, further comprising the step of fabricating the test structure to provide a uniform stress condition on one or more structures.

4. The method as recited in claim 1, wherein the step of building includes employing a dual damascene process.

5. The method as recited in claim 4, wherein the step of building includes forming the dual damascene structure with vias having conductive liners along bottoms and sidewalls of the vias.

6. The method as recited in claim 1, wherein the step of building a test structure includes providing a mismatch in a coefficient of thermal expansion (CTE) between metal and dielectric materials.

7. The method as recited in claim 1, wherein the step of building includes building the test structure to provide a bimodal failure distribution having early and late fails during thermal cycle testing.

8. The method as recited in claim 7, wherein the step of evaluating reliability is based on early fails.

9. A method for evaluating reliability of a semiconductor chip structure built by a manufacturing process, comprising the steps of:

building a test structure in accordance with a manufacturing process, which uses materials having mismatches in coefficients of thermal expansion, the test structure including features having predetermined strain values;

thermal cycling the test structure to induce changes or failures of the features;

measuring the yield of the features in the test structure; and

evaluating reliability of the semiconductor chip structure built by the manufacturing process based on the yield.

10. The method as recited in claim 9, wherein the yield includes a relative number of electrically functional features formed by the manufacturing process before thermal cycling.

11. The method as recited in claim 9, further comprising the step of fabricating the test structure to

provide a uniform stress condition on one or more of the features.

12. The method as recited in claim 9, wherein the step of building includes employing a dual damascene process to form the features.

13. The method as recited in claim 12, wherein the step of building includes forming dual damascene features with vias having conductive liners along bottoms and sidewalls of the vias.

14. The method as recited in claim 9, wherein the step of building a test structure includes providing a mismatch in a coefficient of thermal expansion (CTE) between metal and dielectric materials.

15. The method as recited in claim 9, wherein the step of building includes building the test structure to provide a bimodal failure distribution having early and late fails.

16. The method as recited in claim 15, wherein the

step of evaluating reliability is based on early fails.

17. A test structure used to determine reliability performance, comprising:

a patterned metallization structure having a plurality of interfaces, which provide stress risers;

a dielectric material surrounding the metallization structure, where a mismatch in coefficients of thermal expansion (CTE) between the metallization structure and the surrounding dielectric material exist such that a thermal strain value is provided to cause failures under given stress conditions as a result of CTE mismatch to provide a yield indicative of reliability for a manufacturing design.

18. The structure as recited in claim 17, wherein the same strain value is across all vias in the test structure.

19. The structure as recited in claim 17, wherein the patterned metallization structure includes a dual damascene structure.

20. The structure as recited in claim 17, further comprising conductive liners along bottoms and sidewalls of

vias in the dual damascene structure.

21. The structure as recited in claim 20, wherein the liners include one of tantalum (Ta), tantalum nitride (TaN), titanium (Ti), titanium nitride (TiN) and tungsten (W).

22. The structure as recited in claim 17, wherein the metallization structure includes one of aluminum (Al), copper (Cu), Gold (Au), silver (Ag) and alloys thereof.

23. The structure as recited in claim 17, wherein the dielectric material includes an organic material.

24. The structure as recited in claim 17, wherein the dielectric material includes one of SiLK (trademark of Dow Chemical), polyamide, SiCOH, a nitride and an oxide.

25. The structure as recited in claim 17, wherein the mismatch in CTE between the metallization structure and the dielectric material is greater than about 20ppm/°C.

26. The structure as recited in claim 17, wherein the

metallization structure includes a stacked via chain having at least two levels of interconnects and vias.

27. The structure as recited in claim 17, further comprising dummy structures not electrically connected to the metallization structure and placed near ends of the test structure to reduce the variation in thermal strain at corner or end vias.

28. The structure as recited in claim 17, wherein the metallization structure is separated from metal pads by a distance to reduce thermal expansion effects caused by the metal pads.

29. The structure as recited in claim 28, wherein the distance between the metallization structure and the bond pads is such that a reduction in thermal strain of any via is within 5% of a maximum value of thermal strain that exists between the metallization structure and the dielectric material for a completely isolated via.

30. The structure as recited in claim 17, wherein the metallization structure further comprises multiple sections

electrically connected and separated by a distance to reduce thermal expansion effects caused by adjacent vias.

31. The structure as recited in claim 30, wherein the distance between the sections is such that a reduction in thermal strain of any section is within 5% of a maximum value of thermal strain that exists between the metallization structure and the dielectric material for a completely isolated section of vias.